What is claimed is:

1. An alarm mechanism, comprising:

a hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of at least one alarm and the second register adapted to store current states of each of the at least one alarm; and

a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers.

2. The alarm mechanism of claim 1, wherein the first and second registers comprise first and second n-bit registers for monitoring n alarms.

3. The alarm mechanism of claim 1, and further including a monitoring circuit adapted to monitor serial lines on the backplane of an access device of a telecommunications network to detect alarm conditions and to report alarm conditions to the hardware component.

4. The alarm mechanism of claim 1, wherein the second register is adapted to store a first value for a first state and second value for a second state.

5. The alarm mechanism of claim 4, wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state.

6. The alarm mechanism of claim 1, wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm indicator.

7. An alarm mechanism, comprising:

at least one alarm;

a first register, responsive to the at least one alarm, and adapted to store a value that indicates a change in state of at least one alarm; and

a second register, responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm.

8. The alarm mechanism of claim 7, wherein the at least one alarm comprises an alarm for a serial line on the backplane of an access device.

9. The alarm mechanism of claim 7, wherein the first and second registers comprise first and second n-bit registers for monitoring n alarms.

10. The alarm mechanism of claim 7, and further including a monitoring circuit adapted to monitor serial lines on the backplane of an access device of a telecommunications network to detect alarm conditions and to report alarm conditions to the hardware component.

11. The alarm mechanism of claim 7, wherein the second register is adapted to store a first value for a first state and a second value for a second state.

12. The alarm mechanism of claim 11, wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state.

13. The alarm mechanism of claim 7, wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm indicator.

14. A method for monitoring alarm conditions, the method comprising:
receiving an indication of a change in state of an alarm;
recording the change in state of the alarm in a first register;
recording the current state of the changed alarm in a second register; and
generating an interrupt.

15. The method of claim 14, wherein receiving an indication of a change in state of an alarm comprises receiving an indication of an alarm condition in a serial line on a backplane of an access device.

16. The method of claim 14, wherein recording the change in state comprises recording a first logic value in a bit location of the first register.

17. The method of claim 14, wherein recording the current state comprises recording a first logic value in a bit location of the second register.

18. The method of claim 14, wherein receiving an indication of a change in state of an alarm comprises receiving an indication of an alarm condition when at least two cells are received on communication line with corrupted synchronization patterns.

19. A telecommunications system, comprising:

at least one access device having a plurality of ports adapted to couple to a plurality of subscriber lines;

a plurality of line cards disposed in the at least one access device and providing the plurality of ports;

a monitoring circuit disposed in the access device, the monitoring circuit adapted to monitor for alarm conditions for the at least one access device; and

an alarm mechanism, communicatively coupled to the monitoring circuit, the alarm mechanism including:

a hardware component, including first and second registers, the first register adapted to store a value that indicates a change in state of at least one alarm and the second register adapted to store current states of each of the at least one alarm, and

a software component, responsive to interrupt requests from the hardware component, adapted to read the first and second registers.

20. The telecommunications system of claim 19, wherein the access device comprises a multimedia channel bank.

21. The telecommunications system of claim 19, wherein the access device comprises a digital loop carrier.

22. The telecommunications system of claim 19, wherein the monitoring circuit comprises a monitoring circuit that monitors serial lines on the backplane of the access device.

23. The telecommunications system of claim 19, wherein the line cards comprise at least one of Plain Old Fashion Telephone Service (POTS), digital subscriber line (DSL), and Integrated Services Digital Network (ISDN).

24. The telecommunications system of claim 19, wherein the first and second registers comprise first and second n-bit registers.

25. The telecommunications system of claim 19, wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state.

26. The telecommunications system of claim 19, wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm.

27. An alarm mechanism for a telecommunications access device, comprising:

at least one alarm associated with each of a plurality of serial low voltage differential signal (LVDS) lines of the access device;

a first n-bit register, responsive to the at least one alarm and adapted to store a value that indicates a change in state of the at least one alarm;

a second n-bit register, responsive to the at least one alarm, and adapted to store current states of each of the at least one alarm; and

wherein corresponding bits of the first and second n-bit registers are associated with a corresponding alarm and a corresponding LVDS line.

28. The alarm mechanism of claim 27, wherein the second register is adapted to store a first logic value for an alarm state and a second logic value for a non-alarm state.

29. The alarm mechanism of claim 27, wherein the first register is adapted to store a first value in a bit location of the first register upon one or more changes in state of the corresponding alarm indicator.

30. A method for monitoring alarm conditions in an access device, the method comprising:

monitoring a plurality of serial lines on a back plane of the access device;

when successive cells have corrupted synchronization patterns, generating an alarm;

receiving the alarm;

recording a change in state of an alarm in a first n-bit register;

recording the current state of the changed alarm in a second n-bit register; and

generating an interrupt for a software component to read the first and second n-bit registers.

31. The method of claim 30, wherein receiving an alarm indicator comprises receiving an indication of an alarm condition in a serial line on the backplane of an access device.

32. The method of claim 30, wherein recording a change in state comprises recording a first logic value in a bit location of the first n-bit register.

33. The method of claim 30, wherein recording the current state comprises recording a first logic value in a bit location of the second n-bit register.

34. The method of claim 30, wherein receiving the alarm comprises receiving an indication of an alarm condition when at least two cells are received on communication line with corrupted synchronization patterns.